Design Review 2:   
We created and simulated a model for the entire SRAM. It uses OCEAN and design variables to adjust the size of various elements so we can sweep the block size and number of blocks. I HIGHLY RECOMMEND FUTURE GROUPS START HERE. Understand our model and apply it to your design (and hopefully improve it). Professor Calhoun did not like our decoder models since they don't vary depth with number of blocks/rows/columns. We simulated without them, and then added them to the few best sizes to optimize the SRAM size. In the model,

* b = number of blocks, ba = number of block address bits (log2(b))
* c = number of columns, ca = number of column address bits (log2(c/32))
* r = number of rows, ra = number of row address bits (log2(r))

We also created butterfly plots and Monte Carlo plots to determine the optimal VDD for active and sleep modes.